Course Code: 19EC0409 **R19**

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY :: PUTTUR
Siddharth Nagar, Narayanavanam Road – 517583

QUESTION BANK (DESCRIPTIVE)

Subject with Code: LDICA (19EC0409) **Course & Branch**: B.Tech – ECE

Year &Sem: II-B.Tech & II-Sem **Regulation:** R19

UNIT –I
OP AMP CHARACTERISTICS AND LINEAR APPLICATIONS

1	**a)**	Explain the operation of an Instrumentation amplifier with neat sketch.	[L2][CO2]	**[8M]**
	b)	Discuss about Virtual ground.	[L3][CO1]	**[4M]**
2	**a)**	Discuss about DC and AC characteristics of an ideal OP-AMP with relevant expressions.	[L2][CO1]	**[6M]**
	b)	Differentiate Open-Loop & Closed Loop Op Amp Configurations.	[L3][CO1]	**[6M]**
3		Draw the circuit and explain the working of the following.		
	a)	Voltage to current converter.	[L3][CO2]	**[6M]**
	b)	Current to voltage converter.	[L3][CO2]	**[6M]**
4	**a)**	Describe about the block diagram of Op-Amp.	[L1][CO1]	**[8M]**
	b)	Write the features of 741 op-amp.	[L3][CO1]	**[4M]**
5	**a)**	Illustrate the Ideal Differential Amplifier with Differential mode gain and Common mode gain expressions.	[L3][CO1]	**[8M]**
	b)	Define and explain about Common Mode Rejection Ratio.	[L1][CO1]	**[4M]**
6	**a)**	Analyze the expression of Inverting Amplifier and draw its input and output Wave forms.	[L4][CO1]	**[8M]**
	b)	List out the applications of Comparator.	[L1][CO2]	**[4M]**
7		Draw and analyze the expressions of the following.		
	a)	Differentiator.	[L4][CO2]	**[6M]**
	b)	Integrator.	[L4][CO2]	**[6M]**
8		Explain about the following.		
	a)	Inverting A.C Amplifier.	[L2][CO2]	**[6M]**
	b)	Non-Inverting A.C Amplifier.	[L2][CO2]	**[6M]**
9	**a)**	Explain about the operation of sample and hold circuit with relevant Waveforms.	[L2][CO2]	**[6M]**
	b)	Discuss about Schmitt trigger with neat sketches.	[L3][CO2]	**[6M]**
10		Explain the followings with neat sketch.		
	a)	Inverting Mode comparator.	[L3][CO2]	**[6M]**
	b)	Non-Inverting Mode Comparator.	[L3][CO2]	**[6M]**

Course Code: 19EC0409 **R19**

UNIT –II
ACTIVE FILTERS, OSCILLATORS & TIMERS

1	**a)**	Explain the operation of Astable multivibrator using 555 timer and also derive the expression for frequency of oscillation.	[L2][CO2]	**[8M]**
	b)	Write the application of multivibrator.	[L1][CO2]	**[4M]**
2	**a)**	With the help of schematic diagram explain how 555 timer can be used as Monostable multivibrator.	[L2][CO2]	**[8M]**
	b)	Draw the pin diagram of 555 timer.	[L1][CO2]	**[4M]**
3	**a)**	Design Wien bridge oscillator using op-amp and explain its operation.	[L4][CO2]	**[8M]**
	b)	Define Oscillator and List out the types of the oscillators.	[L1][CO2]	**[4M]**
4	**a)**	What is the principle operation of RC phase shift oscillator? Explain its operation.	[L2][CO2]	**[8M]**
	b)	What are the disadvantages of RC phase shift oscillator.	[L1][CO2]	**[4M]**
5	**a)**	Draw the circuit of a 1^{st} order low pass Butterworth filter and discuss its transfer functions.	[L2][CO1]	**[8M]**
	b)	Compare the low pass and high pass filters.	[L1][CO1]	**[4M]**
6	**a)**	Explain the functional block diagram of 555 timers.	[L2][CO2]	**[8M]**
	b)	Draw the frequency response curve for a band-pass filter.	[L1][CO1]	**[4M]**
7	**a)**	Design the first order high pass filter and discuss its frequency responses.	[L2][CO1]	**[8M]**
	b)	Define Filter and Illustrate the Types of filters.	[L1][CO1]	**[4M]**
8	**a)**	Draw and Explain narrow band pass filter and discuss its frequency responses.	[L2][CO1]	**[8M]**
	b)	Design wide band pass filter.	[L2][CO1]	**[4M]**
9	**a)**	Draw the circuit diagram of the wide Band-Reject Filter and explain its operation.	[L2][CO1]	**[8M]**
	b)	Compare Band pass and Band-Reject Filter.	[L2][CO1]	**[4M]**
10	**a)**	Discuss about All pass filter with neat sketch.	[L2][CO1]	**[8M]**
	b)	Write the equations of narrow Band-Reject Filter.	[L2][CO1]	**[4M]**

Course Code: 19EC0409 **R19**

UNIT –III
PHASE LOCKED LOOPS, CONVERTERS & CMOS LOGIC

1	**a)**	Draw and Explain about the block schematics of PLL.	[L2][CO3]	**[8M]**
	b)	Define PLL and List the applications of PLL.	[L3][CO2]	**[4M]**
2	**a)**	Draw and Explain about the Monolithic IC 565.	[L2][CO3]	**[6M]**
	b)	Draw and Explain about the Basic IC Voltage Regulators.	[L2][CO3]	**[6M]**
3	**a)**	Draw and explain the weighted resistor DAC.	[L1][CO3]	**[6M]**
	b)	Explain about ladder type DAC.	[L1][CO3]	**[6M]**
4		Draw and explain about R-2R DAC with an example.	[L1][CO3]	**[12M]**
5		Explain about counter type ADC with neat block diagram.	[L2][CO3]	**[12M]**
6	**a)**	The basic step of a 9-bit DAC is 10.3 mV. If "000000000" represents 0V. What output is produced if the input is "101101111"?	[L1][CO3]	**[6M]**
	b)	Explain about flash type ADC.	[L2][CO3]	**[6M]**
7		Draw and explain successive approximation type ADC with an Example.	[L1][CO3]	**[12M]**
8		Draw the circuit diagram of Dual Slope ADC and explain its working with neat sketches.	[L1][CO3]	**[12M]**
9	**a)**	Draw the circuit diagram of basic CMOS gate and explain its operation.	[L3][CO5]	**[6M]**
	b)	Compare CMOS, TTL and ECL logic families.	[L5][CO5]	**[6M]**
10	**a)**	Discuss about low voltage CMOS and Interfacing.	[L2][CO5]	**[6M]**
	b)	Explain in detail about basic ECL logic circuit.	[L2][CO5]	**[6M]**

Course Code: 19EC0409 **R19**

UNIT –IV
HARDWARE DESCRIPTION LANGUAGES

1	**a)**	Explain the various data types supported by VHDL. Give the necessary examples.	[L2][CO6]	**[6M]**
	b)	Explain about VHDL program structure.	[L2][CO6]	**[6M]**
2	**a)**	Explain about functions and procedures with an example.	[L2][CO6]	**[6M]**
	b)	Explain about libraries and packages.	[L2][CO6]	**[6M]**
3	**a)**	Discuss about behavioral design element with an example.	[L4][CO6]	**[6M]**
	b)	Design the logic circuit and write a data-flow style VHDL program for the following function. F (P) = ΣA, B, C, D (1,5,6,7,9,13) + d (4,15).	[L6][CO6]	**[6M]**
4		Draw and explain in detail about VHDL design flow.	[L3][CO6]	**[12M]**
5	**a)**	Write about structural design elements with an example.	[L2][CO6]	**[6M]**
	b)	Write a VHDL entity and Architecture for the following function. F(x) = (a + b) (c.d) Also draw the relevant logic diagram.	[L2][CO6]	**[6M]**
6		Design the logic circuit and write VHDL program for the following function. F(X) = Σ A, B, C, D (0, 2, 5, 7, 8, 10, 13, 15) + d (1, 6, 11).	[L6][CO6]	**[12M]**
7		Design the logic circuit and write VHDL program for the following function. F(Y) = Π A, B, C, D (1, 4, 5, 7, 9, 11, 12, 13, 15).	[L6][CO6]	**[12M]**
8		Design a logic circuit for 4-bit parallel adder and write the VHDL code in structural style by considering full adder as a component.	[L6][CO6]	**[12M]**
9		Explain in detail different modeling styles of VHDL with suitable examples.	[L2][CO6]	**[12M]**
10	**a)**	What is the importance of time dimension in VHDL and explain.	[L2][CO6]	**[6M]**
	b)	Explain the behavioral design elements of VHDL.	[L2][CO6]	**[6M]**

Course Code: 19EC0409 **R19**

UNIT –V

COMBINATIONAL & SEQUENTIAL LOGIC DESIGN PRACTICES

1	**a)**	Design a 4 to 16 decoder with 74×138 IC's.	[L6][CO7]	**[6M]**
	b)	Write a VHDL program for the above design.	[L2][CO7]	**[6M]**
2	**a)**	Design a Full adder with Half adder's logic circuit.	[L6][CO7]	**[6M]**
	b)	Write VHDL code for the above design in structural model.	[L2][CO7]	**[6M]**
3	**a)**	Explain the operation of standard IC for 3X8 decoder with necessary truth table and internal architecture.	[L2][CO7]	**[6M]**
	b)	Write a VHDL code for the above Decoder	[L2][CO7]	**[6M]**
4	**a)**	With the help of logic diagram explain 74×157 multiplexer.	[L2][CO7]	**[6M]**
	b)	Write a VHDL code for the above IC in data flow style.	[L2][CO7]	**[6M]**
5		Design a priority encoder that can handle 32 requests. Use 74×148 and required discrete gates. Provide the truth table and explain the operation.	[L6][CO7]	**[12M]**
6	**a)**	Draw the logic symbol of 74 x 85, 4-bit comparator and write a VHDL code for it.	[L3][CO7]	**[6M]**
	b)	Design a 16-bit comparator using 74×85 ICs.	[L6][CO7]	**[6M]**
7	**a)**	Distinguish between the synchronous and asynchronous counters.	[L4][CO7]	[6M]
	b)	Design an 8-bit serial in and parallel out shift register.	[L6][CO7]	[6M]
8	**a)**	Distinguish between latch and flip flop. Show the logic diagram for both. Explain the operation with the help of function table.	[L4][CO7]	**[6M]**
	b)	Write a VHDL code for a D-flip flop in behavioral model.	[L2][CO7]	**[6M]**
9	**a)**	Design a synchronous 4-bit up counter.	[L6][CO7]	**[6M]**
	b)	Write a VHDL code for the above design.	[L2][CO7]	**[6M]**
10		Design an 8 -bit serial in and serial out shift register and write a VHDL cod for it.	[L6][CO5]	**[12M]**

Prepared by:

1. **Mrs. J JHANSI** **Associate Professor/ECE**
2. **Mr. U SRINIVASULU** **Associate Professor/ECE**
3. **Mr K D MOHANA SUNDARAM** **Associate Professor/ECE**